REMARKS

Favorable reconsideration of this application is respectfully requested.

Addressing first the objection to claims 12-15 and 20 noted in paragraph 4 of the Office Action, those claims are amended by the present response as suggested in the Office Action to address the objection thereto.

Claims 1-11, 13, and 15-19 are pending in this application. Claims 12, 14, and 20 are canceled by the present response without prejudice. Claims 1-20 were rejected under 35 U.S.C. § 102(e) as anticipated by U.S. patent 7,020,854 to Killian et al. (herein "Killian"). That rejection is traversed by the present response as discussed next.

Each of the independent claims is amended by the present response to clarify features recited therein. Independent claim 1 now specifically clarifies the at least one of the plurality of option instructions selected is "provided in general-purpose language selected from among RTL description, behavior level description, and C/C++ model description". The other independent claims are similarly amended as in independent claim 1. Those claims features were previously recited for example in dependent claims 12, 14, and 20, and thus the claims amendments do not raise any issues that would preclude entry of the present response.

The claim features are believed to clearly distinguish over the applied art.

The claims as written are directed to allowing efficient design in the field of semiconductor intellectual property. In respect to semiconductor intellectual property, being able to efficiently reuse existing designs can provide an important advantage, particularly as many semiconductor intellectual properties have been designed in HDL such as VHDL and Verilog.

One feature realized by the claimed inventions is to utilize user defined instructions in general-purpose language for designing a processor core. Such a structure makes it possible to reuse existing HDL resources. Particularly, user defined instructions are typically

described in two languages, RTL description and behavior level description or C/C++ model description. The use of a RTL description enables optimized RTL description after high level synthesis. The use of behavior level description or C/C++ model description enables rapid regeneration of a software environment.

With the claimed inventions the user defined instruction in general-purpose language enhances reusing existing HDL resources in a semiconductor design environment.

In maintaining the rejection based on Killian, the outstanding Office Action states:

> Killian et al teaches... designer-defined instructions using TIE instructions, which being flexible describe portion of the ISA and might be called general-purpose language as shown in the examples in the table (col. 14, ll. 19-61), wherein TIE code is related to C language (col. 27, ll. 13-19; col. 30, ll. 55-58; col. 30, ll. 43-46).[1]

In reply to that basis for the rejection applicants respectfully submit the interpretation noted above is inappropriate from a viewpoint of the technical meaning of the term "general-purpose language" recited in the claims.

In Killian all the user defined instructions have the same format and operand usage in accordance with Tensilica Instruction Set Extensions (TIE) codes (see for example Killian at column 16, lines 23-40). In Killian the semantics specified via the TIE instructions can be translated to functionally equivalent C functions. However, in Killian there is no disclosure to the translation from C functions to TIE instructions, i.e., Killian does not disclose or suggest the opposite direction of translation from TIE instructions to C instructions. Applicants submit this is generally true in the case of general-purpose language including RTL description, behavior level description, and C/C++ model description. Applicants note that even if one wants to use a certain intellectual property available in general-purpose

[1] Office Action of March 16, 2006, page 3, lines 12-15.

language, that cannot be realized in the system of Killian because the Killian system allows extension only by TIE instructions, which are a proprietary language.

In contrast to Killian, in accordance with the claimed invention the user defined instructions are described in ***general-purpose language*** selected from RTL description, behavior level description, or C/C++ model description. Killian does not disclose or suggest such features.

As noted above, much semiconductor intellectual property has been designed in RLT description or HDL such as VHDL and Verilog. Such semiconductor intellectual property cannot be reused in the system of Killian, and as a result the development period cannot be shortened by accessing the existing intellectual property in the system of Killian.

In contrast to Killian, in the present invention a plurality of option instructions are provided by description in a general-purpose language. In other words, for example, only by making use of existing VHDL semiconductor intellectual property, with the present invention a processor can be designed with option instructions corresponding to the existing VHDL intellectual property. Killian is in contrast to such a benefit available by the present invention as in Killian any existing VHDL semiconductor intellectual property would have to be rewritten into TIE instructions for use in the system of Killian.

As one non-limiting example, option instructions can be designed by the C language, and corresponding VHDL codes are prepared. The C language codes can be used for implementing a software environment such as a simulator. Such a process may be easy and effective because of the versatility of the C language. However, in the case of Killian, the TIE instructions are translated into the C language from which a simulator may be implemented. Alternatively, a simulator may be implemented directly from the TIE instructions. However, in either way in Killian compilation of a simulator is not as easy compared to a compilation such as in the present invention.

In summary, in contrast to Killian, in accordance with the claimed invention user defined instructions are described in general-purpose language selected from RTL description, behavior level description, or C/C++ model description.

The system of Killian has a drawback that is overcome by the present invention in that the system of Killian cannot efficiently reuse existing designs for semiconductor intellectual property, for example that have been designed in HDL such as VHDL and Verilog.

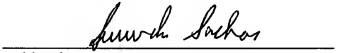
The claimed invention allows reusing existing HDL resources because user defined instructions are described in a general-purpose language. Killian does not disclose or suggest the features clarified in the claims, and Killian cannot realize the benefits in the claimed invention.

In view of the foregoing comments applicants respectfully submit the claims as written distinguish over Killian.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Surinder Sachar
Registration No. 34,423

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 03/06)
EHK/SNS:sjh

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